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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,133	04/25/2006	Hazuki Okabayashi	P29835	8197

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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/577,133	OKABAYASHI ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/21/06, 6/6/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/577,133 has a total of 10 claims pending, there are 2 independent claims and 8 dependent claims.

INFORMATION CONCERNING THE OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

2. Applicant's claim for the benefit of prior-filed application 2003-387351 in the Japanese Patent Office on November 18, 2003 under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged.

INFORMATION CONCERNING DRAWINGS

Drawings

3. Applicant's drawings submitted April 25, 2006 are accepted for examination.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

4. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statements dated July 21, 2006 and June 6, 2007 are acknowledged by the

Examiner and the cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by the Examiner is attached to the instant Office action.

5. The information disclosure statement filed September 15, 2006 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

OBJECTIONS

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "A CACHE MEMORY AND METHOD FOR CACHE ENTRY REPLACEMENT BASED ON MODIFIED ACCESS ORDER"

7. The abstract of the disclosure is objected to because the numerical references "39" and "40" should be removed from the abstract. Correction is required. See MPEP § 608.01(b).

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 2, and 7-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Arimilli et al. (U.S. Patent 6,397,298) (hereinafter "Arimilli").

10. **As per claim 1**, Arimilli discloses a cache memory which holds, for each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the order, the cache entry holding unit data for caching, said cache memory comprising:

a modification unit operable to modify the order data regardless of an actual access order (col. 4, lines 23-31; Fig. 2, element 24; col. 3, lines 36-37; Fig. 1, element 15);

and a selection unit operable to select, based on the modified order data, a cache entry to be replaced (col. 4, lines 12-15; col. 3, lines 36-37; Fig. 1, element 15). *It*

should be noted that a "cache line" is analogous to a "cache entry." It should also be noted that the "least-recently-used (LRU)" cache line is replaced.

11. **As per claim 2**, Arimilli discloses said modification unit includes:

a specifying unit operable to specify a cache entry that holds data which is within an address range specified by a processor (col. 4, lines 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15); *It should be noted that the address in cache where the linefill occurs is analogous to the "address range specified."*

and an oldest-ordering unit operable to cause the order data of the specified cache entry to become oldest in order, regardless of the actual order (col. 4, lines 61-65; col. 3, lines 36-37; Fig. 1, element 15). *It should be noted that the linefilled cache line can be given an access status of "LRU" which would mean it becomes "oldest" in order.*

12. **As per claim 7**, Arimilli discloses said modification unit is operable to modify the order data so that one cache entry shows Nth in the access order (col. 4, lines 61-65; col. 3, lines 36-37; Fig. 1, element 15), and N is any one of: (a) a number indicating the oldest in the access order (col. 4, lines 61-65); (b) a number indicating the newest in the access order; (c) a number indicating Nth from the oldest in the access order (col. 4, lines 61-65); and (d) a number indicating Nth from the newest in the access order (col. 4, lines 61-65). *It should be noted that status "LRU" is analogous to "oldest in the access order", status "LRU+N" is analogous to "Nth from the oldest in the access order", and "MRU-N" is analogous to "Nth from the newest in the access order."*

13. **As per claim 8**, Arimilli discloses said modification unit has:

an instruction detection unit operable to detect that a memory access instruction that includes a modification directive for the access order has been executed (col. 4, lines 23-24 and 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15); *It should be noted that a "linefill operation" is analogous to a "memory access instruction that includes a modification directive for the access order" because after a linefill the corresponding cache line is always assigned an access status other than MRU.*

and a rewrite unit operable to rewrite the order data for a cache entry that is accessed due to the instruction (col. 4, lines 25-31; col. 3, lines 36-37; Fig. 1, element 15).

14. **As per claim 9**, Arimilli discloses said modification unit includes:

a holding unit operable to hold an address range specified by a processor (col. 3, lines 44-46; Fig. 2, elements 21); *See the citation note for the first limitation in claims 2 above. It should be noted that the "tag fields" hold the addresses for the cache lines.*

a searching unit operable to search for a cache entry that holds data corresponding to the address range held in said holding unit (col. 4, lines 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15); *It should be noted that when a linefill operation occurs it is required the cache lines be searched in order to determine the proper cache line to be updated by the linefill.*

and a rewrite unit operable to rewrite the order data so that the access order of the cache entry searched for by said searching unit is Nth in order (col. 4, lines 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15). *See the citation note for claim 7 above.*

15. **As per claim 10**, Arimilli discloses a control method for controlling a cache memory which holds, in each cache entry, order data indicating an access order, and which replaces a cache entry that is oldest in the order, the cache entry holding unit data for caching, said method comprising:

a modification step for modifying the order data regardless of an actual access order (col. 4, lines 23-31; Fig. 2, element 24); *See the citation note for the first limitation in claim 1 above.*

and a selecting step for selecting, based on the modified order data, a cache entry to be replaced (col. 4, lines 12-15).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Pettey (U.S. Patent 6,021,480).

18. **As per claim 3**, Arimilli discloses said specifying unit has:

a judgment unit operable to judge whether or not there is a cache entry that holds data corresponding to each line address from the start line address to the end line address (col. 4, lines 40-41; Fig. 3, element 32; col. 3, lines 36-37; Fig. 1, element 15). *See the citation note for the first limitation in claim 1 above.*

Arimilli does not disclose a first conversion unit operable to convert a starting address of the address range to a start line address that indicates a starting line within the address range, in the case where the starting address indicates a midpoint in line data;

a second conversion unit operable to convert an ending address of the address range to an end line address that indicates an ending line within the address range, in the case where the ending address indicates a midpoint in the line data.

Pettey discloses a first conversion unit operable to convert a starting address of the address range to a start line address that indicates a starting line within the address range, in the case where the starting address indicates a midpoint in line data (col. 37, lines 9-18; Fig. 75, element 2616); *It should be noted that the "read align logic" is analogous to the "first conversion unit."*

a second conversion unit operable to convert an ending address of the address range to an end line address that indicates an ending line within the address range, in the case where the ending address indicates a midpoint in the line data (col. 37, lines 9-18; Fig. 75, element 2616); *It should be noted that the "read align logic" is also analogous to the "second conversion unit."*

Arimilli and Pettey are analogous art because they are from the same field of endeavor, that being cache memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Pettey's align logic within Arimilli's CPU such that any cache address used by the processor would always be properly aligned to a cache line

boundary because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of reducing system latency by allowing misaligned memory accesses to be corrected by aligning the data transfer with a cache line boundary.

19. **As per claim 4**, the combination of Arimilli/Pettey discloses said oldest-ordering unit is operable to attach, to the order data, an oldest-order flag which indicates that the access order is oldest (Arimilli, col. 4, lines 61-65; col. 3, lines 36-37; Fig. 1, element 15). *See the citation note for the second limitation in claim 2 above.*

20. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Pettey as applied to claim 4 above, and further in view of Robinson (U.S. Patent 5,043,885).

21. Arimilli discloses all the limitations of claim 5 except when a cache miss occurs, in the case where a cache entry that has the oldest-order flag attached is present, said selection unit is operable to select the cache entry to be replaced, and in the case where a cache entry that has the oldest-order flag attached is not present, said selection unit is operable to select a cache entry to be replaced in accordance with the order data.

Robinson discloses when a cache miss occurs, in the case where a cache entry that has the oldest-order flag attached is present, said selection unit is operable to select the cache entry to be replaced (col. 4, lines 53-57), and in the case where a cache entry that has the oldest-order flag attached is not present, said selection unit is

operable to select a cache entry to be replaced in accordance with the order data (col. 4, lines 57-59).

Arimilli and Robinson are analogous art because they are from the same field of endeavor, that being cache memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Robinson's reference count and boundary criteria within Arimilli's CPU because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of improving cache management performance by making replacement decisions also based in part on reference frequencies.

22. **As per claim 6**, the combination of Arimilli/Robinson discloses the cache entry has, as the order data, a 1-bit order flag that indicates whether the access order is old or new (Robinson, col. 4, lines 40-45), and said selection unit is operable to select, to be replaced, the cache entry in which the order flag indicates old, in the case where a cache entry that has the oldest-order flag attached is not present (Robinson, col. 4, lines 57-59).

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-10** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,497,477 (Trull) discloses a method and apparatus called a cache insertion selector for selecting a slot of a memory cache in which to insert data. The access history of a slot is monitored with a single boolean variable called "used recently". A slot is marked as "used recently" when it is accessed. When a new entry is to be inserted, the cache insertion selector of the present invention attempts to select a slot which is not marked as "used recently". If all slots are marked as used recently, the cache insertion selector marks all slots as not used recently and selects one slot. A slot can be specified for unconditional selection. Also, a slot can be precluded from being selected.

2. U.S. Patent 6,266,742 (Challenger et al.) discloses a method for determining whether an uncached object should be cached, and, if so, which objects, if any, should be removed from a cache to make room for the new uncached object.

3. U.S. Patent 6,393,525 (Wilkerson et al.) discloses an LRU with protection method is provided that offers substantial performance benefits over traditional LRU replacement methods by providing solutions to common problems with traditional LRU replacement.

4. U.S. Patent 6,738,865 (Burton et al.) discloses a Method, system, and program for demoting data from cache based on least recently accessed and least frequently accessed data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
September 23, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185